REMARKS/ARGUMENTS

The Office Action dated December 19, 2008, has been received and carefully considered. Currently, claims 1-8, 11-19 and 20 are pending. Claims 1-9 and 11-20 are rejected. In this response, claims 1-9 and 11-20 are amended. No new matter has been added. Entry of the amended claims is respectfully requested.

I. OATH/DECLARATION

Applicant respectfully disagrees that the oath/declaration is defective. This application is a 371 of a PCT. As such, the following rules apply:

- 37 CFR 1.69(b) provides in relevant part that "Unless the text of any oath or declaration in a language other than English is in a form provided by the Patent and Trademark Office or in accordance with with PCT Rule 4.17(iv), it must be accompanied by an English translation..." (emphasis added)
- PCT Rule 4.17(iv) permits "a declaration of inventorship, as referred to in Rule 51*bis*.1(a)(iv)..."
- Rule 51*bis*.1(a)(iv) states that the national law applicable by the designated office may require the applicant to furnish "[any document containing an oath or declaration of inventorship] where the international application designates a State whose national law requires that the national application be filed by the inventor."

Further, the MPEP 1893.01(e) provides that "the requirement for an oath or declaration in compliance with 37 CFR 1.497(a)-(b) will have been previously satisfied if a declaration in compliance with PCT rule 4.17(iv) and executed by all the inventors was submitted within the time limits provided in PCT rule 26*ter*.1 in the international phase."

The current German declaration satisfies Rule 4.17(iv) (which incorporates Rule 51*bis*.1(a)(iv)) by providing a declaration in accordance with German national law. Thus, the current declaration is proper and a new declaration is not required.

II. GENERAL OBJECTIONS TO CLAIMS 1-9, 11-20

On Pages 2-6 of the Office Action, all of the claims are objected to for various reasons. The antecedent basis problem noted in numbered paragraph 3 of the Office Action has been addressed by claim amendment. Numbered paragraph 4 objects to claim 1 on the basis of unclear usage of the terms "semiconductor wafer" vs. "wafer." The claim as amended should be clear now. References to "two wafers" in the body of the claim are referring to the "at least two semiconductor wafers" recited in the preamble.

Regarding numbered paragraph 7, Applicants respectfully disagree that this objection rests upon proper grounds. The claims mentioned (4, 5, and 8; 14, 15, and 18) do not depend from one another.

Regarding numbered paragraphs 6 and 8, the antecedent basis problems have been corrected.

The antecedent basis problems noted in numbered paragraphs 9 and 10 have been addressed.

All of the issues raised in numbered paragraph 11 have been addressed.

Regarding numbered paragraph 12, Applicants respectfully submit that the ambiguities discussed have been remedied by the claim amendment.

Regarding numbered paragraph 13, Applicants respectfully submit that this is not a proper basis for a claim objection.

III. THE INDEFINITENESS REJECTION OF CLAIMS 1-9, 11-19 AND 20

On Pages 6-13 of the Office Action, claims 1-9, 11-19 and 20 are currently rejected under 35 U.S.C. 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding numbered paragraph 14, Claim 1 has been amended to cover at least two wafers. These "at least two wafers" are joined (bonded together), and the two wafers have four surfaces. Two of these surfaces are called "wafers sides" in line 10 of claim 1, and they are the bonding face which is covered with the glass pastes. Thus, two of such sides are bonded together, and thereby the two wafers having the other opposed surfaces are bonded.

Specifically referring to the rejection to the term "structured layers," it is respectfully submitted that this term is a well-known term of art. A layer that is not structured is just a flat layer, and a layer that is structured has a pattern in it. Pattern is guiding the paths for electrically conducting or guiding the paths for electrical isolation. This is generally called in the art a "structured layer". Further, such structured layer is explained in U.S. Pat. No. 6,555,414 to Vanfleteren ("Vanfleteren") (*see* column 6, line 66, starting with a pattern of electrical contact heads, and several times using the technical term "pattern".). Similarly, U.S. Pat. Pub. No. 2003/0170936 to Christensen et al. ("Christensen") refers to such structured layers on page 2, paragraph [015], also using the technical term of a patterned buried oxide.

Applicant respectfully submits that the remaining indefiniteness rejections on pages 9-13 of the Office Action have been overcome through the claim amendments.

IV. THE OBVIOUSNESS REJECTION OF CLAIMS 1-8, 11-18 AND 20

On Page 13 of the Office Action, claims 1-8, 11-18 and 20 are currently rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Vanfleteren in view of U.S. Pat. Pub. No. 2004/0142540 to Kellar et al. ("Kellar"). This rejection is respectfully traversed.

The Office Action, at page 15, acknowledges that "Vanfleteren fails to disclose joining tow semiconductor wafers." This is a major deficieny. If Vanfleteren does not show wafers, it does not show processed semiconductor wafers and it does not show a process for connecting those semiconductor wafers, either processed or not processed. Kellar does not cure this major deficiency.

Kellar uses multiple semiconductor wafer bonding (see paragraph [05]). The Office Action is correct in this aspect. The Office Action could have also noted paragraph [01] of Kellar, where wafer bonding is named and specifically a flexible bladder press is used and three-dimensional stacks are provided.

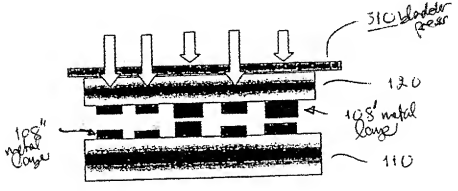
The Office Action interprets claim 1 by saying that what is claimed is any wafer shape, not necessarily semiconductor wafers (see Office Action, page 15, centre paragraph). This is how this paragraph is understood. The semiconductor wafers that are connected are processed semiconductor wafers and they may have electrical structures in them that are to be connected by using said electrically conducting glass paste. The claim describes connecting the wafers not

only by isolating them (*see* Kellar, page 2, paragraph 18 ("while maintaining electrical isolation between active devices of silicon wafers 120, 110, 130")). The claims describe using semiconductor wafers where these wafers were not any wafers, but semiconductor wafers.

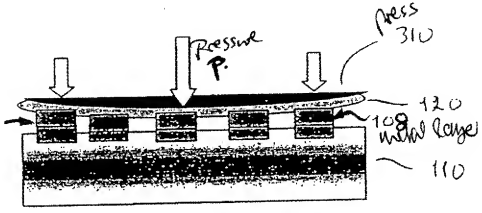
Applying a generalized prior art reference against claims that have been interpreted in an unreasonably broad and generalized manner is improper.

When the term "wafer" is used in the claims (these are the wafers that are mentioned in line 1 of claim 1 and in line 7 of claim 1). They are not generalized; they are said semiconductor wafers that are processed semiconductor wafers. Our wording cannot be clearer, our wording can only be longer, but the scope of the claim would remain the same.

Kellar is shown by the drawings below. The Kellar reference has a metallic layer that is used for bonding and providing electric contact, see page 2, paragraph [023]. These metal bonding layers 108 are in fact the upper layer 108' and the lower layer 108", as shown below from figure 3 of this Kellar document.



Applying force with the certain press 310, will yield a common metal layer 108, as shown in the below drawing, taken from figure 4 of Kellar.



As Kellar says that this bonding layer are copper lines and bumps, they are enhancing the third dimension and providing electrical contact. Why Kellar says that lines and bumps are the same, is not understood here. Shown are bumps that are compressed during pressing action P by press 310. Copper lines only, which are the lines that horizontally interconnect certain areas of activity (electronically structured areas or electric circuit points of these areas, as we have them in claim 7), are not those ones that will yield a metal layer 108 between two opposing surfaces or sides of the two wafers. Copper lines would not be available for vertically compressing, but bumps are available for compressing and electrical connecting between certain stacked layers of which there are two in figures 3 and 4, wafer 110 below and wafer 120 above, to be electrically connected.

Applicants respectfully submit that claim 1 of the present application, using structured layers of non-conducing and electrical conducting glass paste, is taught, suggested, or disclosed by Kellar.

The document of Kellar provides the reader with a prior art history and the typical stack, page 2, paragraph [108], about mid portion with said glass BPSG that maintains electrical isolation. It also provides the reader with an inventive wafer bonding process, page 2, paragraph [023] that has electrical interconnection by copper lines and bumps. The electrical interconnection is not made by glass paste that has different characteristic. We claim this glass paste that is conducting and we claim a glass paste that is non-conducting. Kellar is silent with respect to these two types of glass paste, so this document cannot be used to reject our claims

under USC 103(a). It would not be obvious to remove the metallic layer 108', 108" as taken from figure 3 above. A person of ordinary skill in the art at the time of the invention would not remove this metal layer and replace it by something that is not mentioned in this document. This is hindsight consideration, to actively enforce a replacement in patent terms, that a skilled man in this field of business would not in development terms actually replace or provide. Obviousness test is that something in prior art is reasonably done, and not enforced to be done by the viewer and reader of two certain documents. Applicants respectfully submit that there would have been no reasons whatsoever for a person having ordinary skill in the art at the time of the invention to remove or replace the only new device 108 in said Kellar document by a certain type of non-named electrically conducting glass paste, that would need some temperature with it and not just pressure as the bladder press 310 of this documents suggests. Applicants respectfully submit that neither Kellar nor the knowledge available to a person having ordinary skill in the art would have provided any reasons (or incentives, or motivations, or suggestions, or teachings) to modify either of the cited references in the manner alleged to arrive at the invention recited in claim 1.

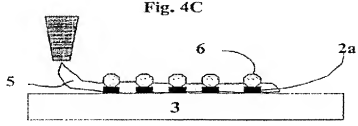
Vanfleteren is silent as to wafers. Vanfleteren is far from wafers as the Examiner actually acknowledges on page 15.

Vanfleteren shows a flip chip assembly that uses bonding as well. Bonding is applied to certain substrates, see claim 1 of this document, column 14, lines 19/20. The flip chip bonding has a plurality of bonding pads, claim 1, line 20. The adhesive used in that claim 1, line 27, is to connect the substrate and keep it connected during drying said adhesive, and curing said adhesive. Where no adhesive is present and where areas are not to be bonded together, an underfill material is used, column 14, line 39 of said claim 1. Still, this whole procedure can only interconnect electrically conducting by using said bonding pads. Whether the adhesive or the underfill material is compared to glass paste is just a further fact at issue. Not the only one.

Criticality in claim 1 is given by using two glass pastes and one of these glass pastes is electrically conducting. Using electrically conducting glass-paste to interconnect is a different type of interconnecting structures, namely our processed semiconductor wafers, than Vanfleteren suggests covers inventive matter.

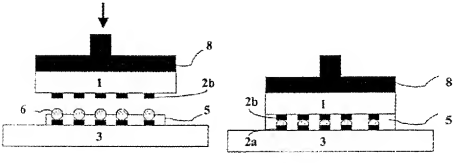
Below are shown figures 4E, 4F of Vanfleteren as an invention. A press applies a force on the bonding pads, and they are deformed. Deforming them is done by pressure only and no relevant temperature is applied. This temperature is used for drying the adhesive, column 8, line 27 and Fig 4C.

Fig. 4C



The curing temperature is below 150°C, much less than used for "curing glass paste". In fact, we are not curing glass, we are melting glass pastes that has a pre-melting step, which is also missing from said type of connecting by bumps 6 in Vanfleteren.

Still, a thermocompression step is used along figure 4F, see column 6, line 55. This thermo part of the compression is in figure 4F, the actual compression happens before, see column 9, line 36 to 50.



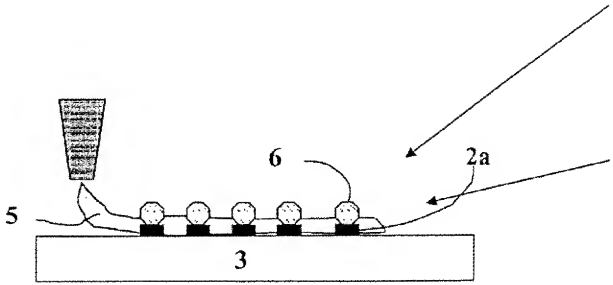
In fact, the use of two types of glass pastes, conducting and non-conducting, the use of a pre-melting step, the alignment and the joining by processing temperatures suitable for melting glass pastes is functionally fully different from what the two references supply.

In fact, the Examiner might use claim 8 of the present application and say that we are using a temperature that is below 450°C and melt the glass pastes, but this is in fact not an upper limit by allowing 5°, 10° or 50° for melting glass pastes, still the melting at said "processing

temperatures of glass paste" itself says that this must be higher than some 100°C and it is in fact according to the description in the range of 450°C, see page 4, third paragraph of English translation of PCT as filed.

Figure 4C of Vanfleteren shows curing and shows the two types of materials that are used and that the Examiner applies on page 17, second paragraph against claim 11, in fact against claim 1 as well, see page 14, first dot in the indented portion (about centre of page). The Office Action alleges that the non-conducting material is the filler material 5 in figure 4C (see column 8, line 48). The Office Action further alleges that the electrically conducting material 6 are the bumps that are applied in figure 4B and that are still present in figure 4C, see column 8, line 45.

Figure 4C is shown below again. The raised bumps 6 and the under bump filling material 5, one of them conducting and providing vertical connection in electrical way, the other one filling the gaps when the pressing action occurs as seen in figure 4F.



It is unfair against claim 1 to apply an unreasonably broad interpretation to the "glass paste" language. A glass paste is not electrically conducting, but it is not the glue or adhesive 5 that is shown in figure 4C. A glass paste does not need to be dried and cured, it is melted and pre-melted. These technical terms are applied to glass pastes, and they are applied according to our claim 1 to two different types of glass pastes, one conducting and the other one isolating.

The Office Action's approach to read the isotropically conducting adhesive (ICA) into the technical term of non-conducting glass paste is not appropriate. The same applies to the bumps 6. The Office Action does not even try to read the electrically conducting bumps as they are shown in Vanfleteren as glass paste. Rather, it is just assumed that they are glass paste. They are not. The reference says in column 8 quite clearly and quite determined that epoxy adhesives are to be used as underfill material and non-conductive adhesives for UV curing can be successfully used for said underfill material 5, see column 8, lines 7 to 12. When or whether such adhesive has a certain "glass temperature", column 11, lines 29/30 is of no concern and does not modify the adhesive to become a glass paste. The matter of drying is a matter of curing or polymerisation, line 33.

The isotropic conducting material is the ICA and is also termed to be some sort of glue or adhesive, see column 7, lines 52 to 55. The conducting material 6, column 8, line 54/55 and the underfill material 5 as NCA are neither glass like nor are they glass pastes. They are of adhesive type and this is what the Examiner can extract from Vanfleteren. The claimed wording excludes adhesive.

To summarize, the claimed functional context of our method claims process semiconductor wafers. It uses two-types of glass pastes and the two types of glass paste are melted at processing temperatures to interconnect vertically and to isolate horizontally and vertically and to serve for tight seals, see page 2, second paragraph from bottom. It is surprising and an astonishing effect the skilled man of wafer bonding would not have expected when applying two types of glass pastes and processing them for melting and firmly connecting in a wafer bonding process. Simultaneously electrical connection can be provided, simultaneously sealing is provided and firmly positioning the two wafers in a relative position.

Also Mori, mentioned on page 18, second paragraph from bottom, would not suggest this. Mori is assumed to be standard technique the Examiner applies, as no certain reference was identified that Mori in fact represents. The inventors supply the following information that they assume that the Examiner mentions contacting by Mori is something that is used in other processes with respect to a PCB contact gap, but they have also mentioned that they are not sure what reference the Examiner wishes to apply in this respect on page 18.

V. THE OBVIOUSNESS REJECTION OF CLAIMS 9 AND 19

On Page 22 of the Office Action, claims 9 and 19 are currently rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Vanfleteren et al. and Kellar et al. as applied to claims 1 and 11 above, and further in view of U.S. Pat. Pub. No. 2003/0170936 to Christensen et al. ("Christensen"). This rejection is respectfully traversed.

The reference the Examiner has generally applied Christensen and specifically page 22 and item (23). This is applied against claim 9 and 19. Claim 9 was withdrawn from consideration, claim 19 as well. They were re-joined now. These claims have prior produced openings for VIAS and might be somewhat related to Christensen, but in fact the more general claims 1, 11 and 20, which are the independent claims, have not been rejected based on Christensen. Christensen does not show the two types of glass pastes and no firm interconnecting of two wafers. Based on the abstract and the figures the Examiner applied on page 22, this document does not deal with anything that relates to a firm interconnection of several wafers by using two types of glass pastes, see specifically figure 6, that exemplifies an insulator and a conductor 600 that is filled into the insulated hole, that is seen in section, see for example page 3, paragraph [027].

The arguments given for support of claim 1 are substantially the same that are used for claims 11 and 20. They have process features that have supported novelty and inventive step of claim 1 over the cited references. We refer to those arguments for these two independent claims 11 and 20 as well.

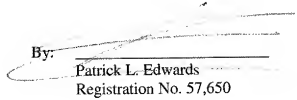
CONCLUSION

In view of the foregoing amendments and arguments, it is respectfully submitted that this application is now in condition for allowance. If the Examiner believes that prosecution and allowance of the application will be expedited through an interview, whether personal or telephonic, the Examiner is invited to telephone the undersigned with any suggestions leading to the favorable disposition of the application.

It is believed that all necessary fees are being charged for filing this Response. However, the Director is hereby authorized to treat any current or future reply, requiring a petition for an extension of time for its timely submission as incorporating a petition for extension of time for the appropriate length of time. Applicant also authorizes the Director to charge all required fees, fees under 37 C.F.R. § 1.17, or all required extension of time fees, to the undersigned's Deposit Account No. 50-0206.

Respectfully submitted,

HUNTON & WILLIAMS LLP



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